CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A structure having an abrupt doping profile comprising:

a single crystal semiconductor substrate having an upper surface,

a first epitaxial layer of Ge over said upper surface,

said first epitaxial layer having a thickness less than the critical thickness,

said first epitaxial layer having a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant selected from the group consisting of phosphorus and arsenic, and

a second epitaxial layer of a semiconductor material over said first epitaxial layer.

2. The structure of claim 1 wherein said second layer comprises a material selected from the group consisting of Si and SiGe.

3. The structure of claim 1 wherein said first layer has a

thickness in the range from 0.5 to 2 nm.

4. The structure of claim 1 wherein said second layer has a concentration change from said first layer into 40Å of said second layer of greater than 1 X 10^{19} atoms/cc.

5. The structure of claim 1 further including a third epitaxial layer of semiconductor material having a doping profile with a dopant concentration less than 5 X 10^{18} atoms/cc.

6. The structure of claim 1 wherein said second epitaxial layer having a thickness of at least 300 Å and having a doping of P less than 5 X 10^{16} atoms/cc for a predetermined thickness after its initial 300 Å thickness.

7. A method for forming an abrupt doping profile comprising the steps of:

selecting a single crystal semiconductor substrate having a major upper surface,

first forming a first epitaxial layer of Ge over said upper surface,

said first epitaxial layer having a thickness less than the critical thickness,

said step of first forming including the step of incorporating a concentration of dopant greater than 5 X 10^{19} atoms/cc, said dopant selected from the group consisting of phosphorus and arsenic, and

second forming a second epitaxial layer of a semiconductor material over said first epitaxial layer.

8. The method of claim 7 wherein said step of selecting includes the step of selecting a plurality of substrates, each substrate having a major upper surface, and wherein said steps of first forming and second forming are performed with respect to said plurality of substrates.

9. The method of claim 7 wherein said step of first forming further includes the steps of placing said substrate in a first CVD reactor and flowing a germanium containing gas and a dopant containing gas.

10. The method of claim 7 wherein said step of first forming further includes the step of adjusting the growth rate of said first epitaxial layer as a function of time.

11. The method of claim 10 wherein said step of adjusting the growth rate further includes the step of changing the flow rate of

said Ge containing gas.

12. The method of claim 7 wherein said step of first forming further includes the step of terminating said step prior to reaching the critical thickness of said first epitaxial layer.

13. The method of claim 7 wherein said step of second forming said second epitaxial layer further includes the steps of placing said substrate in a first CVD reactor and flowing a silicon containing gas and a dopant containing gas, said dopant selected from the group consisting of phosphorus and arsenic.

14. The method of claim 13 wherein said step of second forming further includes the step of adjusting the flow rate of said dopant containing gas as a function of time.

15. The method of claim 7 wherein said step of forming said second epitaxial layer includes after the step of first forming said first epitaxial layer, the steps of removing said substrate from said first CVD reactor to a load lock having a controlled atmosphere to prevent oxidation of the surface of said second layer, and

transferring said substrate to a second CVD reactor having internally exposed surfaces initially free of phosphorus.

16. The method of claim 7 wherein said step of second forming said

second layer includes the steps of removing said substrate from said first CVD reactor to a load lock having a controlled atmosphere to prevent oxidation of the surface,

flowing a silicon containing gas into said first CVD having heated surfaces to coat said heated surfaces with a third silicon containing layer to cover said heated surfaces that may contain phosphorus containing layers that may have formed during the formation of said first epitaxial layer,

transferring said substrate into said first CVD reactor, and

forming a fourth layer on said upper surface of said second epitaxial layer.

17. The method of claim 16 wherein said step of flowing a silicon containing gas includes the step of flowing the combination of $H_2/SiH_4/GeH_4$.

18. A method for forming abrupt doping within a semiconductor layered structure comprising the steps of:

selectively amorphizing a first layer having a high Ge content greater than 0.5, and

crystallizing said amorphized first layer by solid phase

regrowth.

19. The method of claim 18 wherein said step of selectively amorphizing includes the step of ion implantation.

20. The method of claim 18 wherein said step of selectively amorphizing includes first forming second and third layers about said first layer, said second and third layers having a Ge content less than 0.5.

21. The method of claim 18 wherein said step of selectively amorphizing includes the step of first forming said first layer having a Ge content greater than 0.5.

22. A field effect transistor comprising:

a single crystal substrate having a source region and a drain region with a channel therebetween and a gate electrode above said channel to control charge is said channel and

a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic positioned below said channel and extending through said source and drain regions.

23. The field effect transistor of claim 22 wherein said layer of

Ge is in the range from .5 to 2 nm thick.

24. The field effect transistor of claim 22 wherein said channel is in a second epitaxial layer selected from the group consisting of Si and SiGe formed over said first layer.

25. A field effect transistor comprising:

a single crystal substrte,

a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic formed on said substrate,

a second layer of undoped SiGe epitaxially formed on said first layer,

a third layer of strained undoped semiconductor material selected from the group consisting of Si and SiGe,

a source region and a drain region with a channel therebetween, and

a gate electrode above said channel to control charge in said channel.

26. The field effect transistor of claim 25 wherein said layer of

Ge is in the range from 0.5 to 2 nm thick.

27. A field effect transistor comprising:

a single crystal substrate,

an oxide layer formed on said substrate having an opening,

a gate dielectric and gate electrode formed in said opening over said substrate,

a source and drain region formed in said substrate aligned with respect to said gate electrode,

a dielectric sidewall spacer formed on either side of said gate electrode and above a portion of said source and drain regions,

a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic selectively positioned over exposed portions of said source and drain regions,

a second layer of semiconductor material selected from the group consisting of Si and SiGe doped with a dopant selected from the group consisting of phosphorus and arsenic epitaxially formed

over said first layer to form raised source and drain regions.

28. The field effect transistor of claim 27 wherein said layer of Ge is in the range from 0.5 to 2 nm thick.